AN-726
Application Note

BUSSING WITH MECL 10,000 INTEGRATED CIRCUITS

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High speed data bus lines are an important part of modern computer systems. Features of the MECL 10,000 family allow construction of data busses in a transmission line environment. This application note describes some of the guidelines to consider when designing high speed bus lines and shows how the MC10123 can be used for maximum bus performance.

MOTOROLA *Semiconductor Products Inc.*

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INTRODUCTION

A bus line is designed to interconnect several points in a system with a common data path. Normally drivers and receivers are located at each end of the line, so data can flow in either direction. Additional drivers and receivers often connect to the bus at various points along the line, requiring that the driver be capable of sending a signal in both directions. For this reason, a high speed bus driver must operate into a load equal to one-half the line characteristic impedance. Only one driver on a bus can send data at any given time. If more than one MECL driver were simultaneously transmitting, any output at a high logic state would predominate causing a loss of data.

System busses utilize either a single ended or differential operating mode. A differential bus requires two wires per signal path and the receiver looks at the voltage difference between the two lines. The differential line has noise immunity advantages for longer bus runs, but this approach is speed limited when compared to a single-ended bus. A differential system requires special drivers and receivers which are usually slower than high speed logic circuits. Also, present approaches to differential bus driving switch only one line of the differential pair when initializing a data transfer. This results in a crosstalk condition between the two lines which may limit maximum speed.

The single-ended bus uses one wire for each data path, minimizing wire and interconnection requirements. The signal voltages on a single-ended bus are referenced to some common voltage, usually ground, so standard high speed MECL circuits function as both drivers and receivers. With the use of high speed circuits as drivers, performance is largely determined by the transmission line characteristics of the bus. This application note discusses the transmission line parameters which should be considered in the design of a high speed MECL single-ended bus. Some of these parameters include termination, capacitive loading, stub lengths, and timing considerations.

HIGH SPEED SINGLE-ENDED BUSSES

High speed single-ended busses commonly have a high fanout density and use MECL circuits as drivers and receivers. Fanout on a MECL bus is not limited by dc loading considerations, however, circuit input and output capacitance will slow ac performance. Input capacitance of a MECL gate is about 3 pF and output capacitance about 2 pF. With packages soldered in and stray capacitance considered, distributed capacitance averages about 5 pF per circuit connection.

Performance tests were made on a typical MECL bus line as illustrated in Figure 1. This line is a 75-ohm microstrip built on a 0.062 inch double sided G-10 epoxy circuit board. Nine drivers and nine receivers are distributed along the 32-inch line at 4-inch intervals.

A 50-ohm termination resistor is used at each end of the line to minimize reflections. Fanout along a signal line lowers the effective characteristic impedance by the equation:

$$Z_O' = \frac{Z_O}{\sqrt{1 + \frac{C_D}{C_O \ell}}}$$

where

Z_O, the unloaded line impedance = 75-ohms

C_D, the total distributed capacitance = 5 pF per fanout

C_O, the line intrinsic capacitance per unit length = 24 pF per foot for the 75-ohm microstrip line.

ℓ = length of line in inches.

Calculating the characteristic impedance of the bus line in Figure 1 gives:

$$Z_O' = \frac{75}{\sqrt{1 + \frac{90}{24\ (2.67)}}} = 48 \text{ ohms}$$

The two 50-ohm resistors in parallel are a 25-ohm load which is beyond the specified 50-ohm drive of a standard MECL output. For this reason, MC10111 triple output gates are used as bus drivers. These gates have three outputs, each capable of 50-ohm loads. Paralleling two outputs gives the required 25-ohm drive.

Propagation delay time of the bus is a function of the line type, length, and load. Unloaded microstrip line has a propagation delay of 1.77 ns per foot for G-10 circuit board material with a dielectric constant of 5.0. This gives an unloaded propagation delay time of (32 in ÷ 12 in/ft) X 1.77 ns/ft or 4.72 ns for the 32-inch bus line. The unloaded bus model measured 4.92 ns propagation time. The slight increase from calculated time is due to added capacitance from the short stubs and differences in the dielectric constant between the test board and the calculated 1.77 ns per foot.

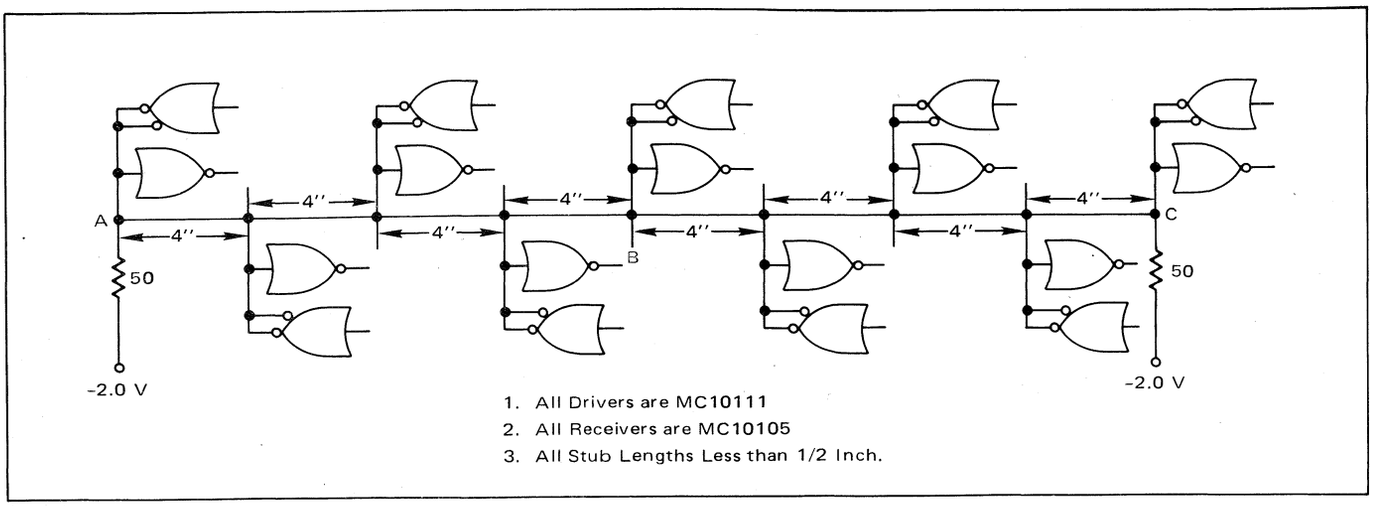

FIGURE 1 – MECL Bus Test Fixture

Propagation delay time of a loaded line may be calculated from the following equation:

$$t_{pd}' = t_{pd}\sqrt{1 + \frac{C_D}{C_{0\ell}}}$$

where t_{pd} is the unloaded line propagation delay. The bus line in Figure 1 loaded only with receiving gates has a calculated delay of:

$$t_{pd}' = 4.92\sqrt{1 + \frac{45}{24\ (2.67)}} = 6.42 \text{ ns}$$

This compares with 6.62 ns for the tested bus line.

When the bus line is loaded with both drivers and receivers, the increased distributed capacitance slows the calculated propagation delay to 7.62 ns. Test waveforms for the bus line in Figure 1 are shown in Figure 2. Propagation delay for a high or low transition is 7.7 ns and agrees with the calculated time. However, the low to high delay is increased to 9.7 ns because of a step in the rising edge of the waveform. This rising edge step is due to the output impedance characteristics of a MECL circuit. When the bus line is at a low logic level, all driver outputs are sourcing current to the termination resistors. These MECL outputs appear as low (7 to 10 ohm) impedances along the line. A rising signal traveling down the bus sees these low impedance outputs and reflects back to the sending point causing the rising edge step. After the signal rises to a level where the nondriving emitter followers are no longer sourcing current, these outputs become high impedances and reflections no longer occur. The transition from high to low is no problem because only the active driver is sourcing current and the other circuits appear as high impedances along the line.

In the preceding example, it was shown that fanout on a bus will lower the characteristic impedance of the line. This should be taken into consideration when determining termination resistor values. A low impedance line is less affected by loading than a higher impedance line. However, since a bus line is terminated at both ends, the driver output current capability must be considered as a limit to minimum line impedance.

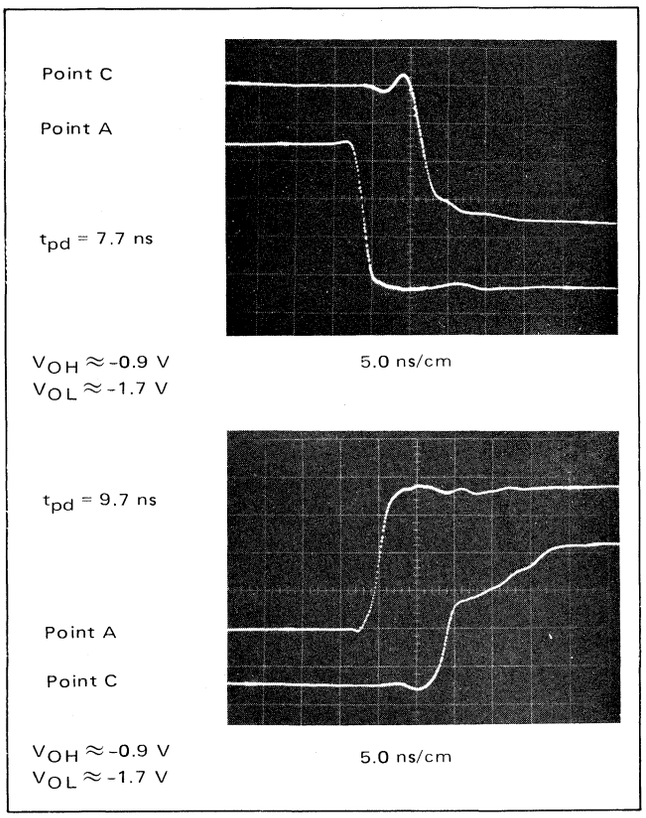

FIGURE 2 – Bus Waveforms With MC10111 Drivers

Standard MECL 10,000 circuits are specified driving a 50-ohm load. This equates to a 100-ohm bus line terminated at each end. Therefore, when these circuits are used as drivers, fanout density must be limited or the line will be overterminated (actual line impedance less than 100 ohms) and reflections will occur. For short bus lengths, typically less than 12 inches, this is acceptable as reflections die out within a few nanoseconds.

Propagation delay increase with fanout must also be considered when figuring bus line performance. Propagation delay is least affected by low impedance lines. Therefore, it is usually desirable to design long bus runs with the lowest impedance line that is compatible with the driver circuits.

For short bus lines the advantage of driving the bus from any MECL circuit and not having special drivers overcomes any delay caused by high impedance lines. With longer busses, the designer has the choice of using a high impedance line with standard circuits or increasing performance by going to a properly terminated lower impedance line. Lower impedance lines require paralleling MECL circuits for increased drive or going to special circuits within the family which have better than 50-ohm drive. The recommended minimum bus line impedance is 34 ohms (17-ohm resistive load) which could be driven by MC10110 or MC10111 circuits having all three outputs wired together. The 50-ohms as in Figure 1 is a more conservative limit.

Ideally, the loading on a bus line should be evenly distributed along the line. With this type loading, the impedance is constant along the line and reflections are minimized. It is realized that in system design this is not always possible and care should be taken to avoid lumping too much capacitance at one point on a long line. For example, if lump loading is held to less than 21 pF in a 7.7-inch length of 68-ohm microstrip line, reflections will be less than 20% along the line. Additional information on lump loading is available in Chapter 7, page 145 of the "MECL System Design Handbook" (Ref. 1). If the loading is evenly distributed on the line, there is no practical limit to fanout density other than minimum line impedance for the driver.

The low impedance outputs of standard MECL circuits cause an impedance discontinuity on the line, and limit rising edge performance of high speed busses. If the bus lines are less than 18 inches, the reflection-caused step in the rising edge is largely hidden in the relatively slow MECL 10,000 rise time and performance degradation is minimal. However, for longer lines, this step in the rising edge will cause a slowing of data transfer which should be considered in the design of a high speed bus system.

THE MC10123 FOR HIGH SPEED BUSSES

When using standard MECL 10,000 circuits as drivers, low impedance discontinuities on the bus line caused a step in the waveform and limit the maximum performance of long bus lines. If the unused outputs could be made to have a high impedance in both the high and low logic states, bus performance would be improved. Since MECL busses are normally terminated with resistors to -2.0 volts, a MECL low logic level below -2.0 volts would turn off the emitter follower output.

The MC10123 is designed with a low logic level specified between -2.03 and -2.10 volts. Therefore, when the bus is at a low level, the line is at the -2.0 termination voltage and all drivers have a high output impedance. A rising edge sees no reflections, so rise time is improved. The primary difference in using the MC10123 as a bus driver is the bus logic levels of -2.0 and -0.9 volts instead of the normal MECL levels of -1.7 and -0.9 volts. Although not necessary or even recommended, the termination voltage could be raised to -1.7 volts and the MC10123 driven bus would have normal MECL levels with no reflections. A second feature of the MC10123 is the 25-ohm drive capability. Busses as low as 50 ohms can be terminated at each end without having to use multiple output driver circuits.

The MC10123 Bus Drivers were substituted for the MC10111's in Figure 1. The results of the MC10123 bus are in the Figure 3 waveforms. When compared with Figure 2, the step in the rising edge is missing with the associated improvement in propagation delay to 7.9 ns.

The oscilloscope photograph of the negative going edge in Figure 3 shows some ringing due to reflections at the driving end of the bus. This is because the driver goes below the termination voltage and becomes a high impedance load. Therefore, any small reflections are not clamped by the low impedance output as was the case in Figure 2. This ringing is not a problem and causes no loss of noise margin because the low level output voltage of the MC10123 bus in Figure 3 is 300 mV more negative than the normal MECL output.

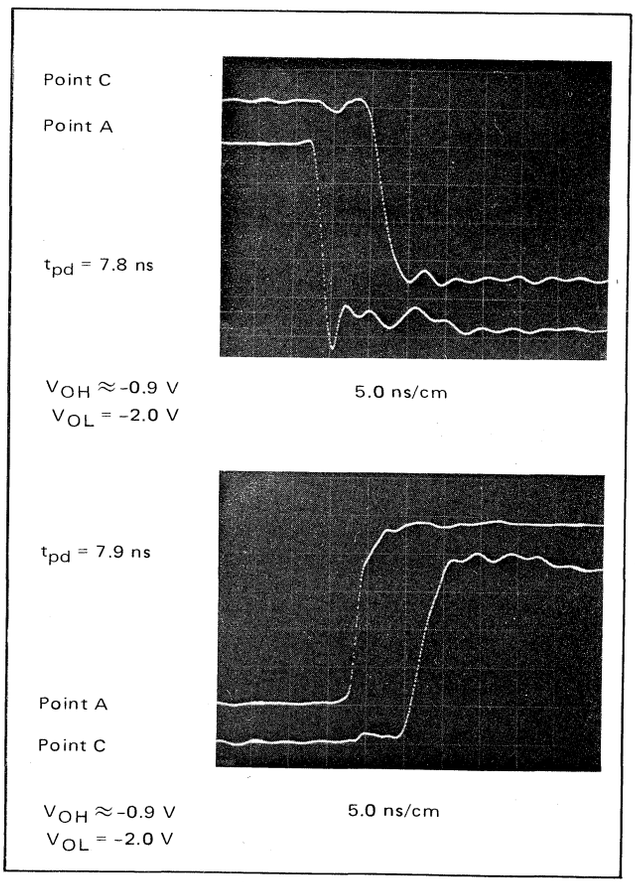

FIGURE 3 – Bus Waveforms With MC10123 Drivers

The advantages of a bus using MC10123 drivers become more apparent when signals along the bus are examined. Figure 4 shows the waveforms for the bus in Figure 1 driven at point A and the oscilloscope monitoring point B. The large step in the rising edge of the MC10111 driven bus is completely eliminated in the MC10123 bus.

The MC10123 bus driver is recommended where maximum performance is required over long line lengths and high fanout. This part minimizes reflections on the bus

line and noticeably improves propagation delay time. However, when maximum speed is not required or lines are kept short, using standard MECL circuits as bus drivers should not be disregarded as this minimizes part count and still gives good system speed.

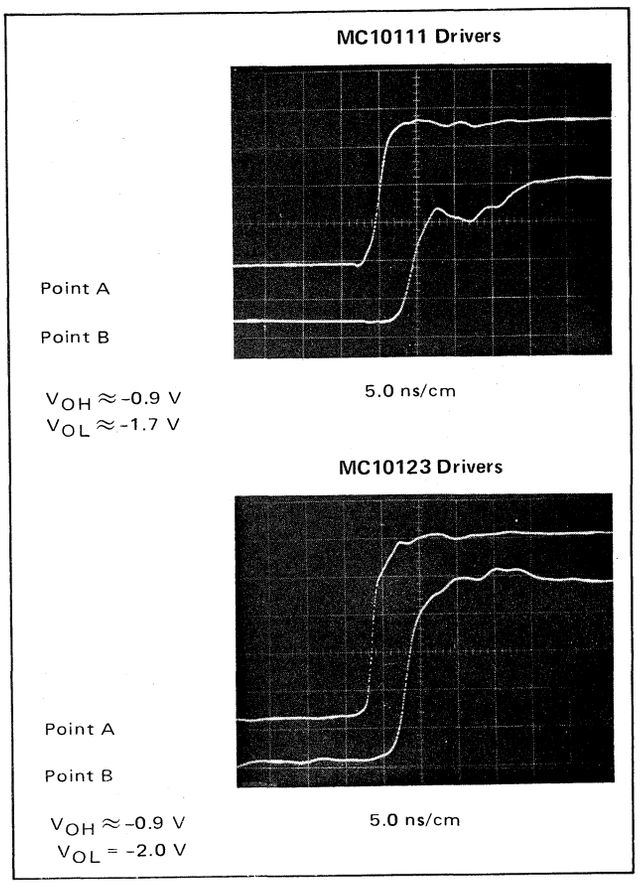

FIGURE 4 – Bus Waveforms at Midpoint

There is no absolute limit to the length of MECL bus lines. Lines of 25 feet and longer are possible if good transmission lines are used to restrict external noise coupling. The delays of these long lines will be significant and should be considered when calculating overall system performance.

STUBBING OFF A MECL BUS

Stubs on a MECL bus should be designed for minimum length. A stub on a bus appears as an impedance discontinuity to a signal on the line, causing a series of reflections. The signal reaching the stub point splits, sending reduced amplitude signals down both the line and the stub. The longer the stub, the greater the time for the reflections to settle out and the signal to reach final amplitude. The primary effect of these reflections is a rounding of the signal edge, resulting in increased propagation delay and decreased bandwidth. By keeping stub lengths short, the reflections are hidden in the signal rise or fall time and high speed performance is maintained.

Reflections and waveforms at points along a bus can be analyzed with a lattice diagram. A lattice diagram shows the amount of signal reflected at discontinuities on a line, allowing waveforms to be calculated. Reflection coefficients are used to determine the amplitude of each reflection. Additional details on lattice diagrams can be found in the "MECL System Design Handbook," Chapter 7, (Ref. 1).

Figure 5 shows a bus being driven from one end (point A), a stub on the bus (points B and C) and a terminated end at point D. The reflection coefficients are calculated from the formula:

$$\rho = \frac{Z1 - Z2}{Z1 + Z2}$$

Where Z1 is the line impedance before the discontinuity and Z2 the characteristic impedance after the discontinuity as seen from the driving source. Figure 5 also shows the reflection coefficients at key points on the bus for a 75-ohm line. A high logic level output impedance of 10 ohms for the MC10123 driver is used in the output high calculations and a very high output impedance is used for the low logic level reflection coefficient. The line will be analyzed for both conditions.

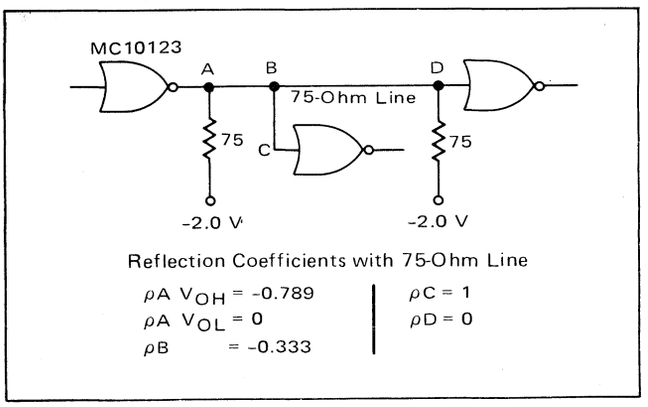

FIGURE 5 – Reflection Coefficients for a Stub on a MECL Bus Line

Figure 6 is the lattice diagram for the bus in Figure 5. Points A, B, C, and D are the four vertical lines. Time is determined by the vertical scale as a function of line and stub propagation delays. This particular lattice diagram was drawn with the stub length B to C much shorter than line A to B to allow the B to C reflections to settle out before the reflections from B to A returned.

Following the lattice diagram, at time 0 a signal leaves point A with an amplitude normalized to 1.0. After propagation delay time A to B, the signal reaches point B. Here the signal sees a discontinuity with a reflection coefficient equal to -0.333. A signal of -0.333 returns down the line from B to A and the difference between the initial signal (1.0) and the reflected signal (-0.333) of +0.667 travels down both lines B to C and B to D. The voltage at point B is also equal to 0.667 of the initial signal. After propagation delay time BC, the signal reaches point C, sees a reflection coefficient of 1.0 and reflects back to B. This returning reflection at B sees a reflection coefficient of -0.333 and reflects back to point C with an amplitude of (0.667) x (-0.333) or -0.222. The difference between 0.667 and -0.222 travels down line B to A and B to D. These reflections between B and C continue, each getting smaller until they die out.

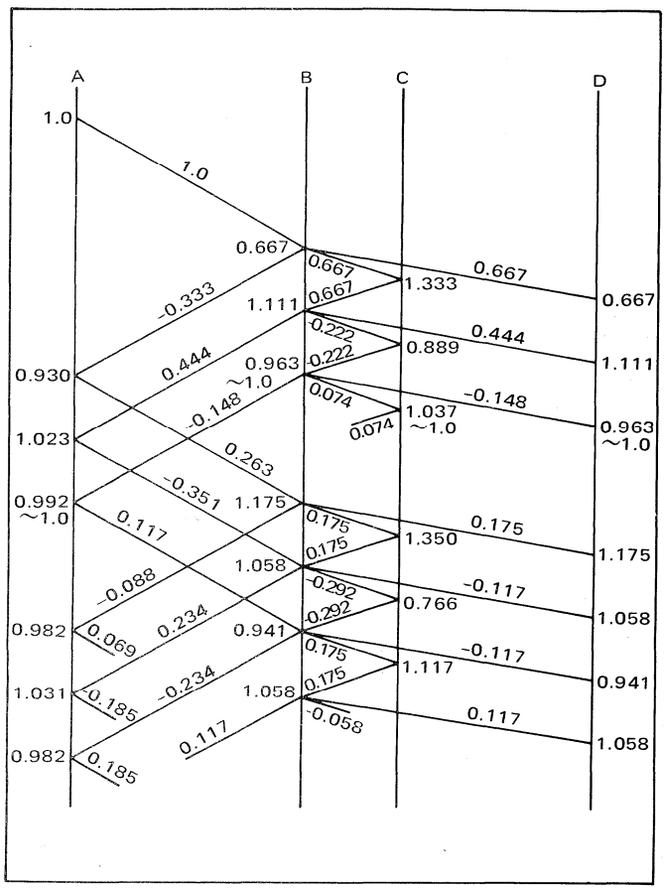

FIGURE 6 – Lattice Diagram for End-Driven Line with Stub

If the driver at point A has a low output level, the line is properly terminated at 75-ohms, no reflections occur and the sequence is terminated. However, if the driver is in a high state, the reflected signal from B to A sees the 75-ohm termination resistor and the MECL output impedance or a reflection coefficient of -0.789. This results in a reflected signal going from A to B delayed in time from the initial signal by twice the A to B propagation delay. This signal, smaller in amplitude than the original signal, causes another series of B to C reflections.

Point D need not be considered from a signal reflection standpoint since this point is always properly terminated. The waveshape at point D is the same as point B delayed in time by one B to D propagation delay.

Plotting the waveforms at A, B, and C, as shown in Figure 7, illustrates the results of reflections on the line. The initial signal ends up with a big step at two-thirds amplitude that results in a greatly increased 10-90% rise time. The increase in rise time would occur at each succeeding stub along the line. Also, a reflected pulse from point A results in a negative pulse along the line that can cause a loss of noise immunity.

A test fixture was constructed with a 12-foot, 75-ohm line between points A and B, a 2-foot stub B to C, and a 4-foot length for B to D. To get a fast signal edge, the line was driven by a pulse generator with 1.0 ns edge speed. The photograph in Figure 8 shows the waveforms at points A, B, and C, and has a very good correlation with the lattice diagram calculations.

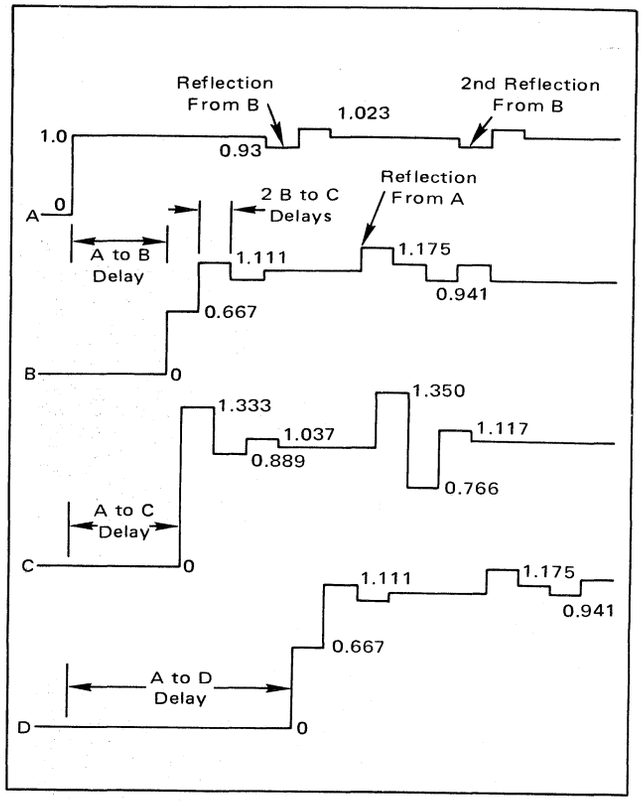

FIGURE 7 – Waveforms of Figure 6 Lattice Diagram

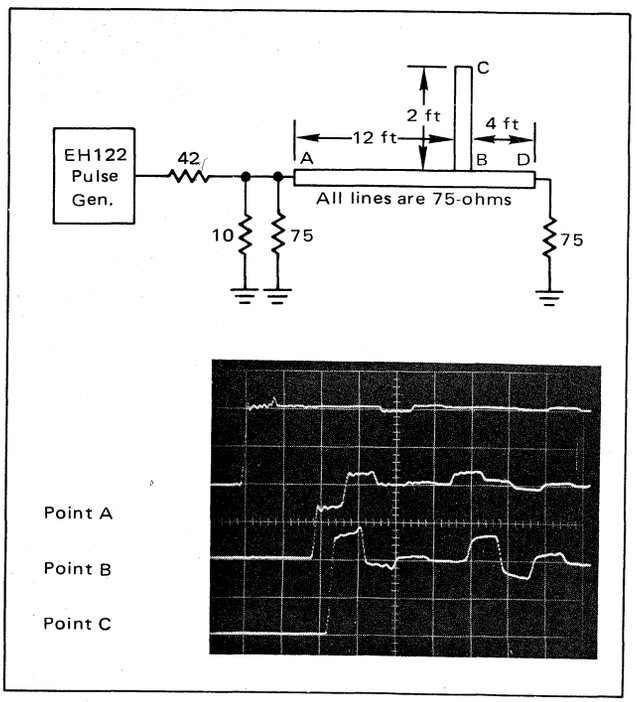

FIGURE 8 – Test Results of a Stub on a Signal Line

In addition to driving a bus from one end as in the previous example, it is necessary to drive from points along the line. This type of bus and the associated lattice diagram are shown in Figure 9. Waveforms at points on the line, Figure 10, point out the slowing of edge speed caused by reflections between points B and C. Unlike the previous example, reflections from the line ends need not be considered since both ends are properly terminated.

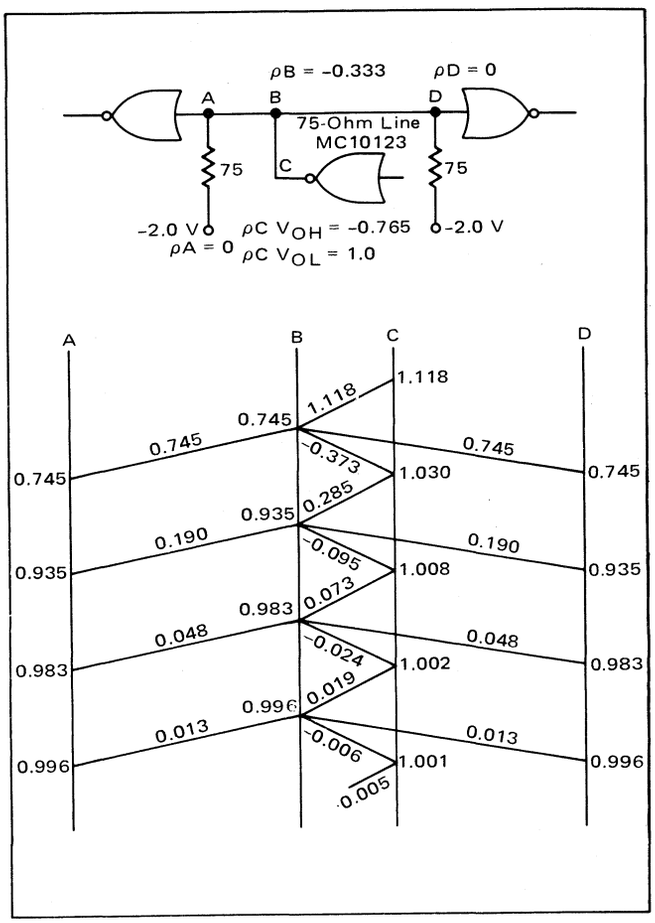

FIGURE 9 – Lattice Diagram for Center-Driven MECL Bus

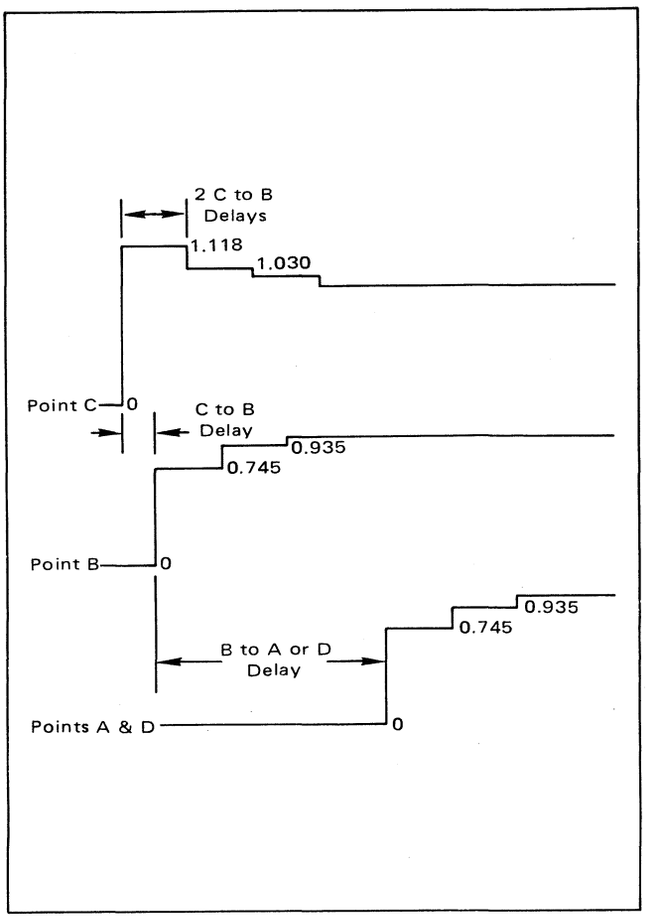

FIGURE 10 – Waveforms of Figure 9 Lattice Diagram

Notice also the initial signal at point C is 1.118. This value was calculated to give a final bus voltage normalized to 1.0. The driving circuit sees a final load of 37.5 ohms and an initial load of only the 75-ohm stub. An output impedance of 10 ohms gives an overshoot of 11.8% at point B which drops to a final value of 1.0 as the reflections die out.

This section using lattice diagrams appears to show that stubs cause a serious loss of edge speed when used in a high speed system. However, this will be true only if the stubs are long with respect to the signal edge speed. If stubs are sufficiently short, the reflections decay very rapidly. For example, a 1-inch stub on microstrip board has a one way propagation delay time of 0.148 ns. This means 5 two-way delay times, normally enough for reflections to settle out, occur within 1.5 ns or about one-half a MECL 10,000 10 to 90% rise time. The waveforms in Figure 3 are for a bus with 14 short stubs. Although there are some minor reflections, the signals will work very well in a MECL system.

There is no strict limit to stub lengths which can be used in a MECL system. If time permits reflections to settle out, long stubs (greater than 6 inches) can be used. However, when top speed is required, stubs will have to be kept shorter. If the bus is restricted to one circuit board, stub lengths can be kept to one-half inch and not be noticed. When the bus is constructed in a system backplane and must fanout to several cards, bus stubs should be restricted to 1.5 to 2 inches. This is sufficient to get through the card connector and to a MECL package near the connector. For these bus runs, it is usually better to have the bus driver and receiver near the edge connector or use buffer gates in place of running long stubs on the circuit board.

CONCLUSION

Although only a few examples have been presented, the techniques described in this application note can be used with a wide variety of bus lengths and fanout densities. The importance of operating in a transmission line environment has been demonstrated by the good correlation between calculations and test results. Using proper termination practices and considering the effects of reflections on a bus line can lead to higher performance and error free operation from a high speed MECL system.

REFERENCES:

1. "MECL System Design Handbook," Motorola Inc., 1972.
2. "MECL Integrated Circuits Data Book," Motorola, Inc., 1973.
3. Defalco, J.A., "Reflections and Crosstalk in Logic Circuit Interconnections," IEEE Spectrum, July, 1970, pp. 44-50.

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